Sequential Circuits

Mechanical and Electrical Engineering

Second Grade Level

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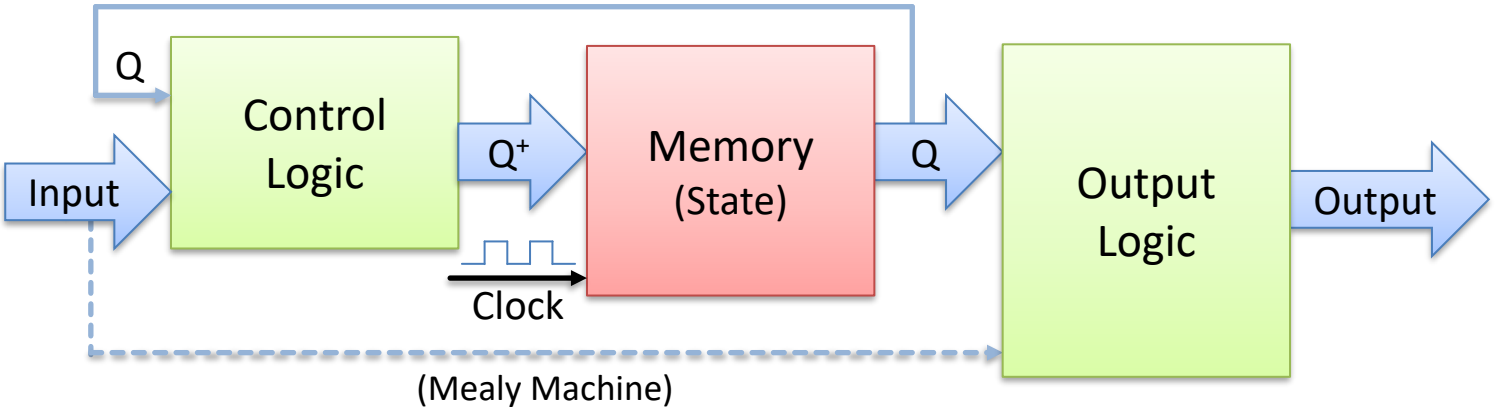
Sequential Circuits (1)

- Two representations are frequently used
  - Mealy Machine (dashed arrow allowed)
  - Moore Machine (dashed arrow not allowed)

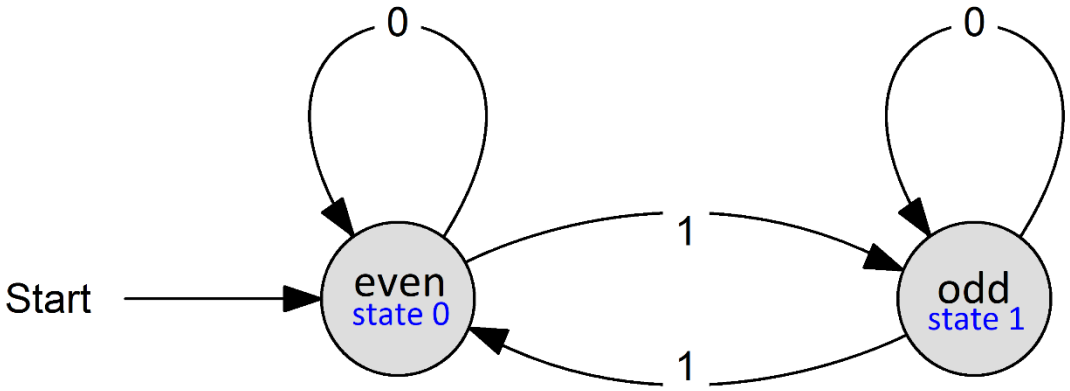


Sequential Circuits (2)

- Design process
  - Create state diagram
    - Number of states
    - Transitions and conditions
  - Encode states
    - One D flip-flops per bit
  - Design control logic
    - State/transition table
  - Design output logic

Sequential Circuits (3)

- Example I
  - Assignment
    Design a sequential circuit which outputs 1 if an even number of 1 was read.
  - State diagram



Sequential Circuits (4)

- Example I (continued)
  - Number of states
    - Even, odd → 2 states → 1 bit → 1 D flip-flop
  - State table (transitions and conditions)

Q	a	Q^+
Even (0)	0	Even (0)
Even (0)	1	Odd (1)
Odd (1)	0	Odd (1)
Odd (1)	1	Even (0)

a Input

Q Current State

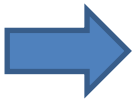
Q^+ Next State

Sequential Circuits (5)

- Example I (continued)
  - Encoding of states
    - Even bit count: 0, 2, 4, 6, …
    - Odd bit count: 1, 3, 5, 7, …
  - Output logic

State	Encoding
Even	0
Odd	1

Q	y
0	1
1	0

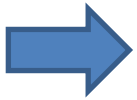


$$y(Q) = \neg Q$$

Sequential Circuits (6)

- Example I (continued)
  - Control logic

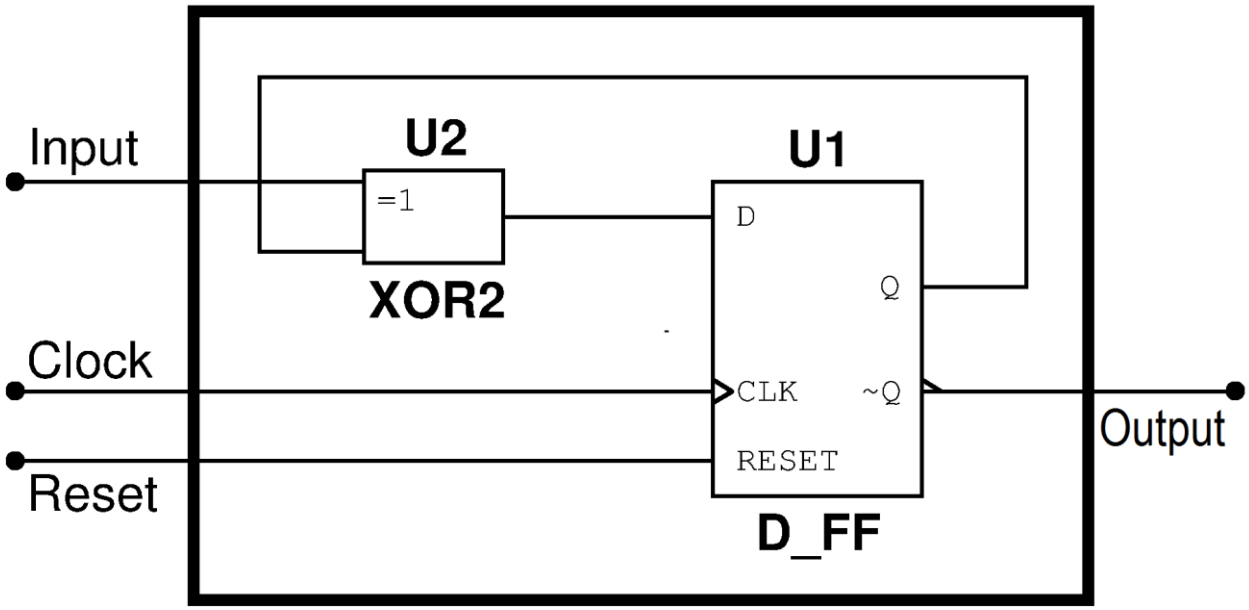
Q	a	Q^+
0	0	0
0	1	1
1	0	1
1	1	0



$$Q^+ = Q \oplus a$$

Sequential Circuits (7)

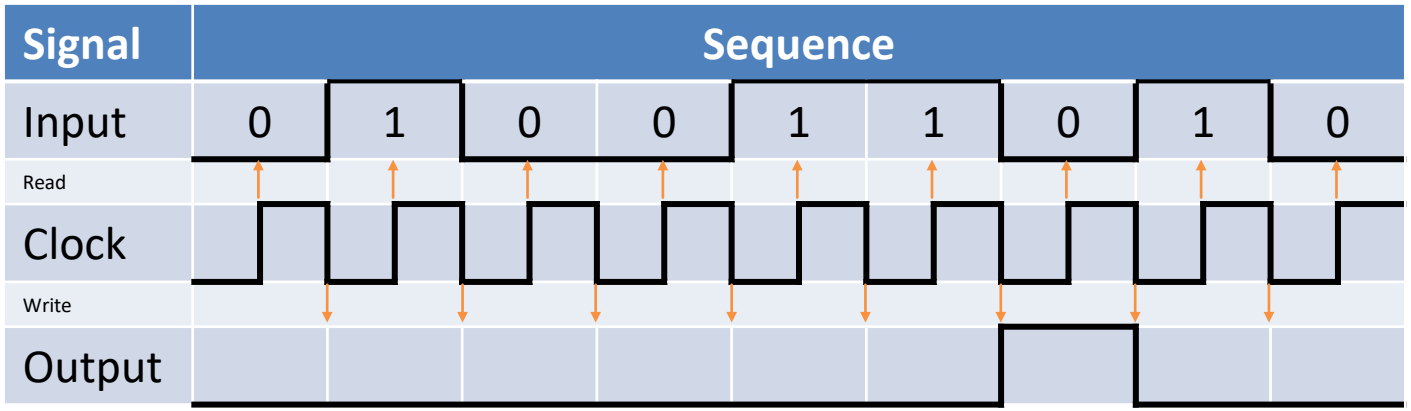
- Example I (finished)
  - The resulting sequential circuit



Sequential Circuits (8)

- Example II
  - Assignment

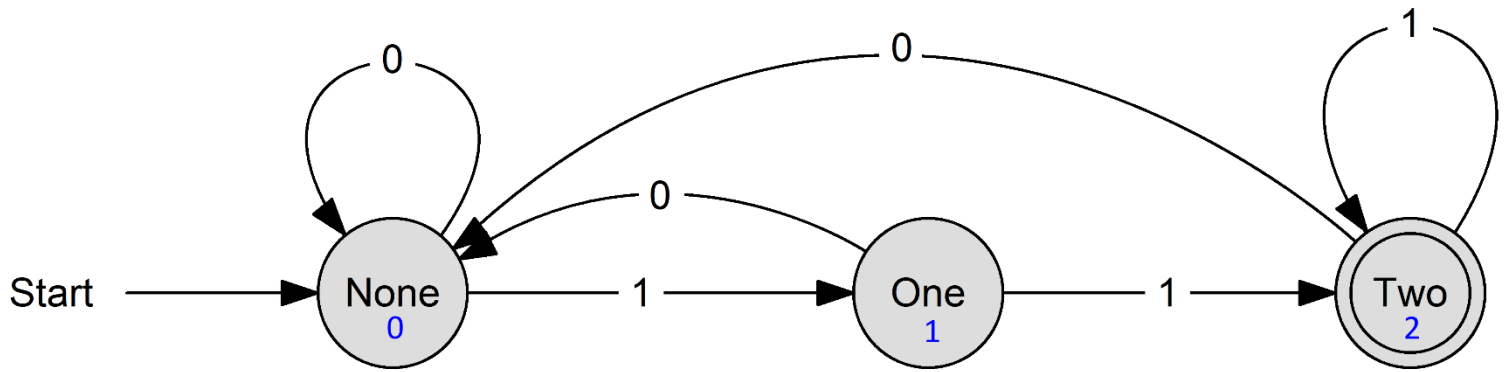
    Find two subsequent *1* in a bit sequence



Pulse Diagram

Sequential Circuits (9)

- Example II (continued)
  - Number of states
    - None, one, two ones → 3 states → 2 bits
  - State diagram



Sequential Circuits (10)

- Example II (continued)
  - Control logic

Q_1	Q_0	a	Q_1^+	Q_0^+
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	X	X
1	1	1	X	X

State	Encoding
None	0 → 0 0
One	1 → 0 1
Two	2 → 1 0

$$Q_0^+ = a \wedge \neg Q_0 \wedge \neg Q_1$$
$$Q_1^+ = (a \wedge Q_1) \vee (a \wedge Q_0)$$

Sequential Circuits (11)

- Example II (finished)
  - Output logic

Q_1	Q_0	y
0	0	0
0	1	0
1	0	1
1	1	X

$$y = Q_1$$