Shift Registers

Networks and Embedded Systems

First Grade Level

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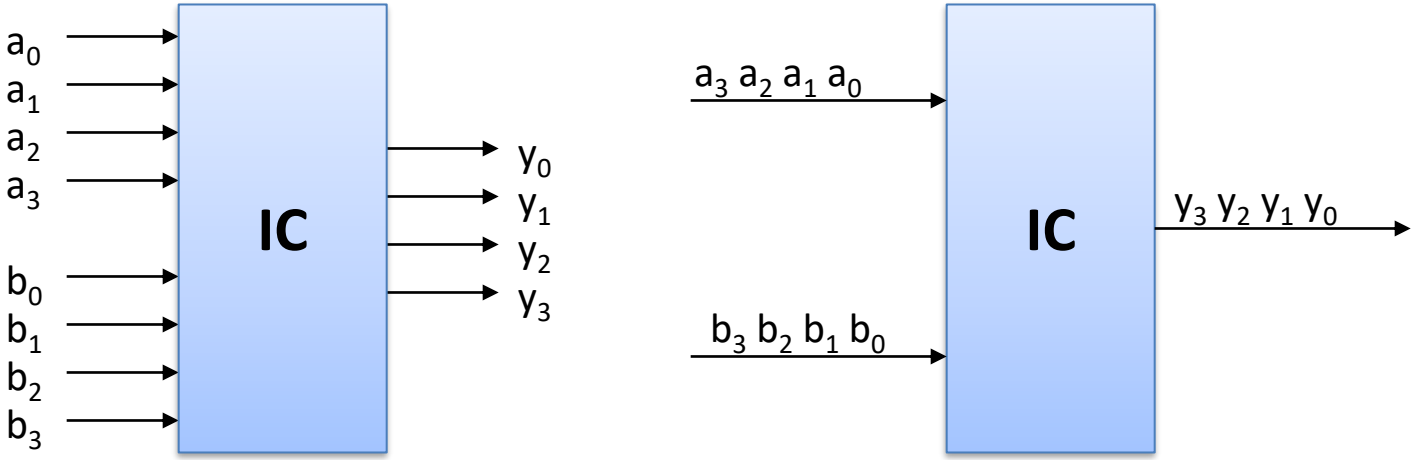
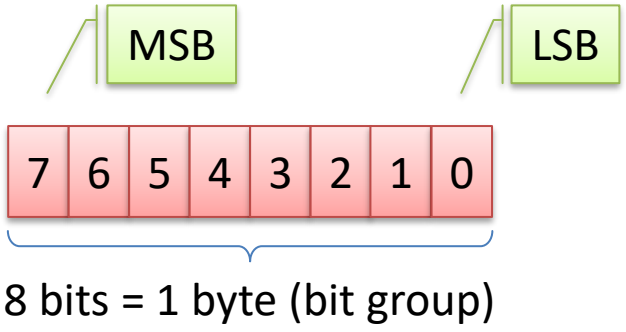
Serial and Parallel (1)

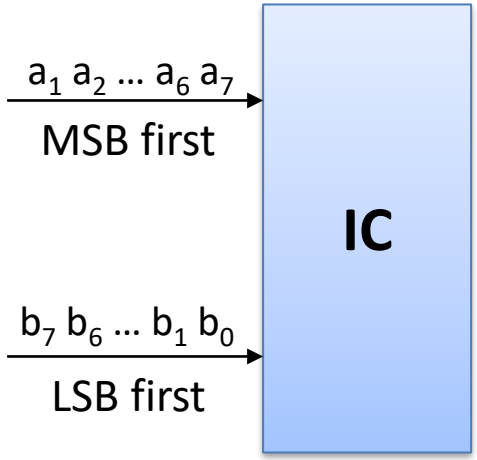
- Parallel vs. Serial
  - Bits can come in parallel or in series
    - Parallel: all at a time, a group of bits
    - Serial: one after another, a series of bits



Serial and Parallel (2)

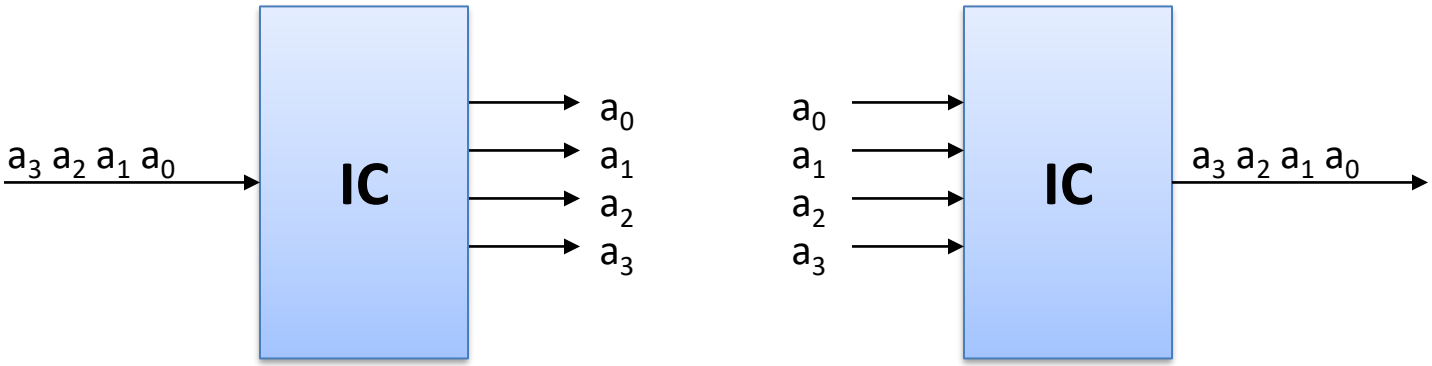
- MSB or LSB First
  - Bits can come in different orders
    - Most significant bit (MSB) first
    - Least significant bit (LSB) first





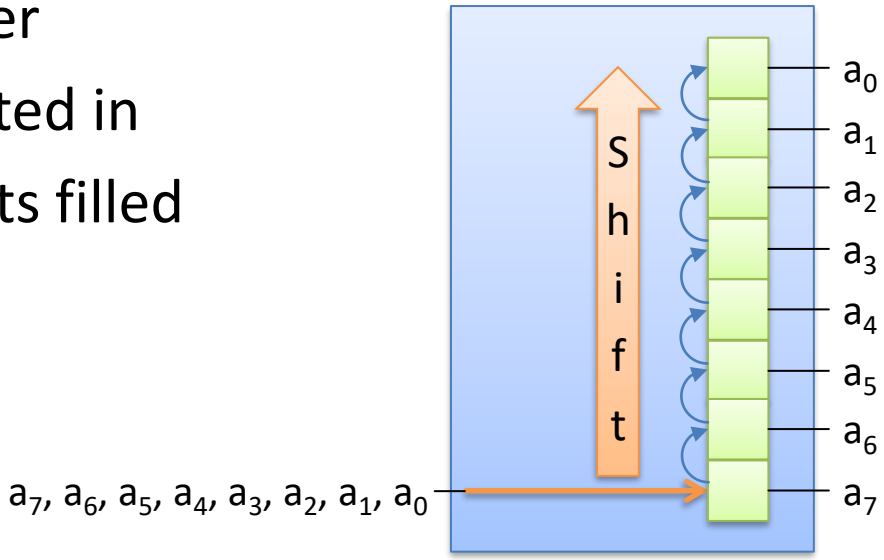
Serial and Parallel (3)

- Converter
  - Serial-to-parallel converter
    - A series of bits is converted into a bit group
  - Parallel-to-serial converter
    - A bit group is converted into a series of bits



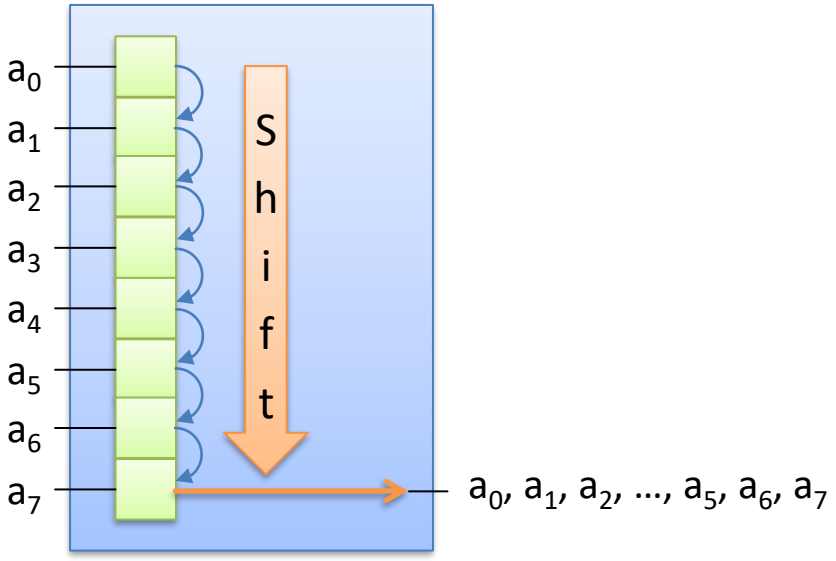
Serial and Parallel (4)

- Serial-to-Parallel Converter
  - Implementation
    - Shift register
    - Data is shifted in
    - Register gets filled



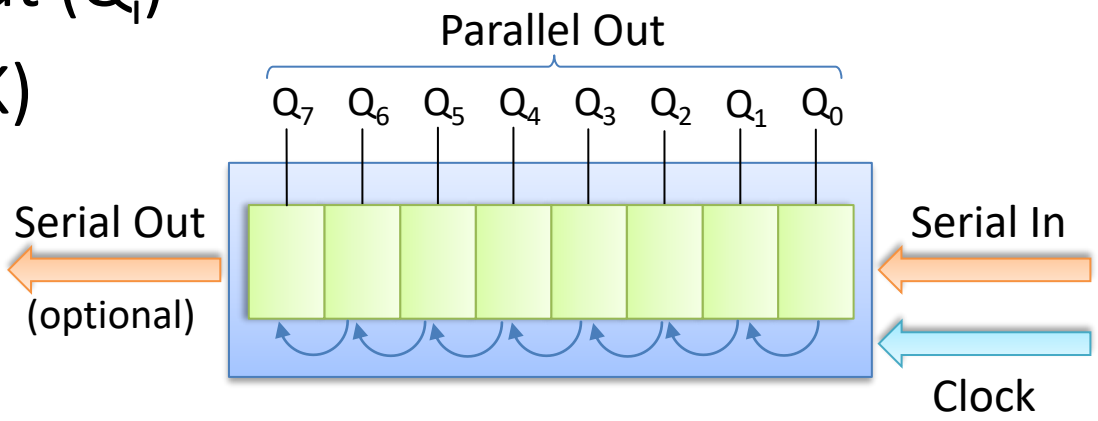
Serial and Parallel (5)

- Parallel-to-Serial Converter
  - Implementation
    - Shift register
    - Data is shifted out
    - Register gets empty



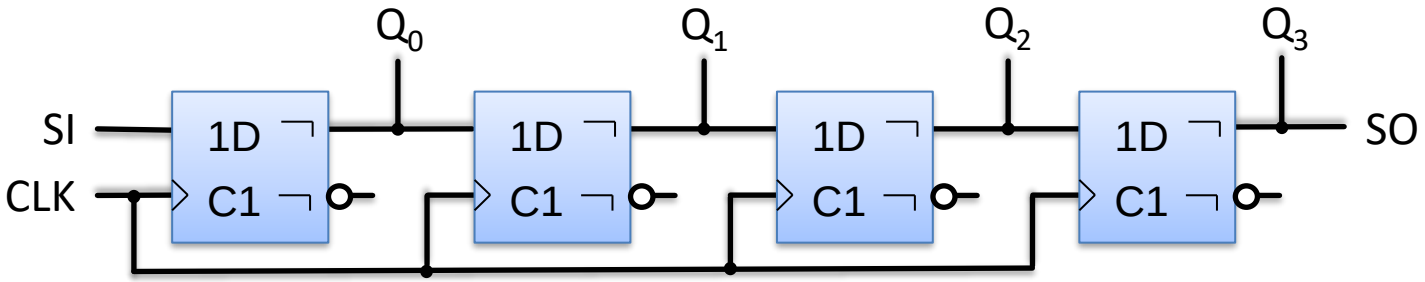
Shift Registers (1)

- Mode of Operation
  - Serial in (SI), Data in (DIN, DI)
  - Serial out (SO)
  - Parallel out (Q_i)
  - Clock (CLK)



Shift Registers (2)

- Mode of Operation (continued)
- Implementation
  - D flip-flops
  - Daisy chain
  - Common clock



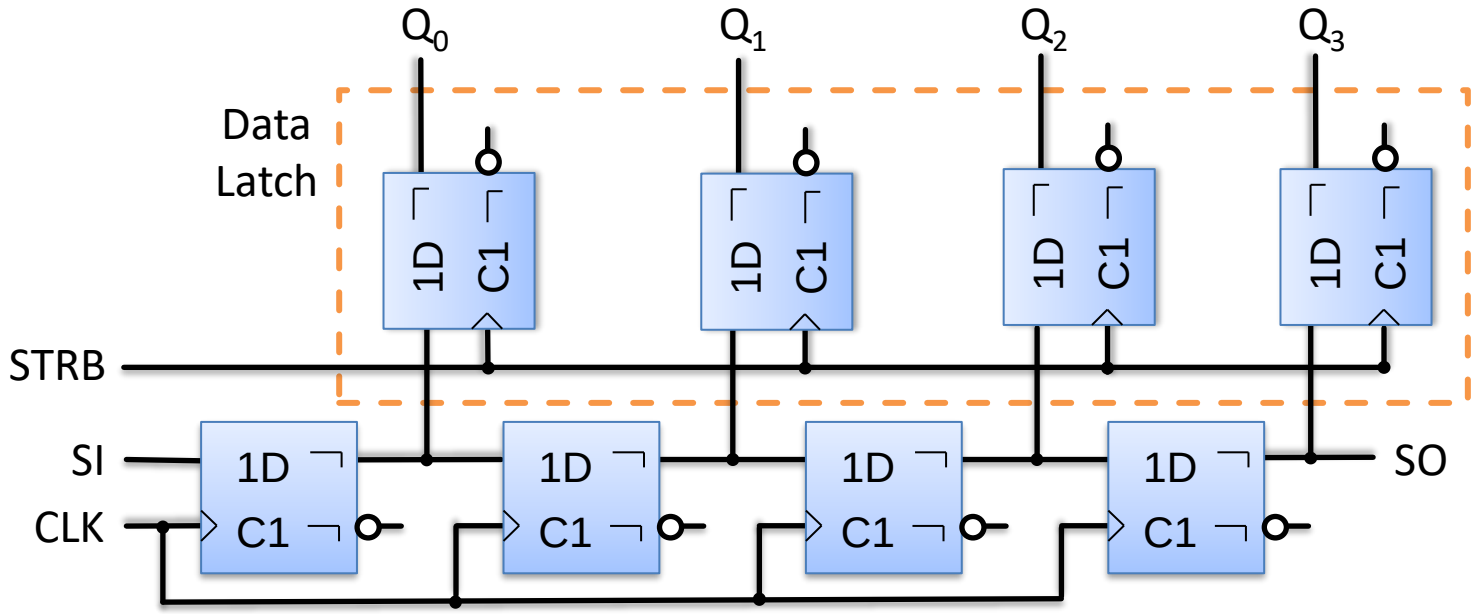
Shift Registers (3)

- Mode of Operation (finished)
  - Demonstration: shifting a bit

Tick	SI	CLK	Q_0	Q_1	Q_2	Q_3	SO
0	0	↑	0	0	0	0	0
1	1	↑	0	0	0	0	0
2	0	↑	1	0	0	0	0
3	0	↑	0	1	0	0	0
4	0	↑	0	0	1	0	0
5	0	↑	0	0	0	1	0
6	0	↑	0	0	0	0	1
7	0	↑	0	0	0	0	0

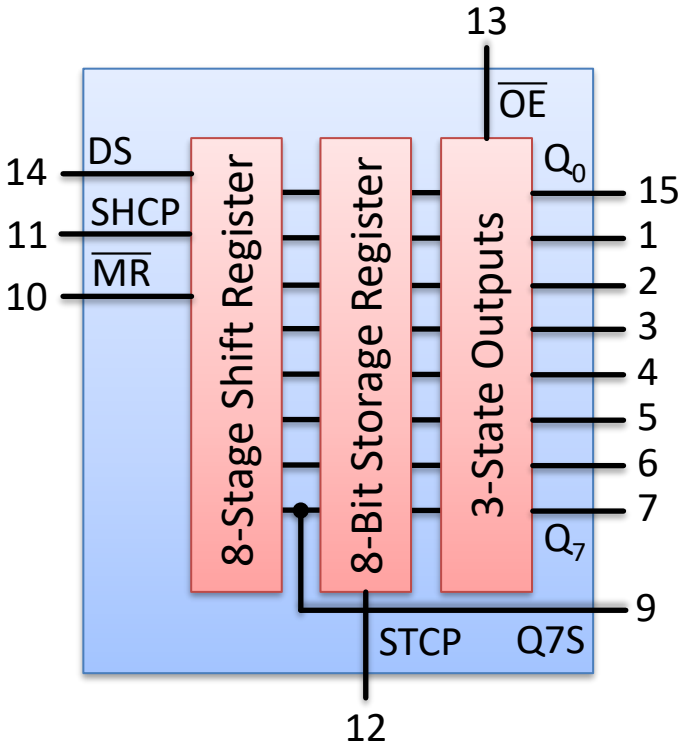
Shift Registers (4)

- Output Latches
  - Hide the process of shifting
  - Strobe activates latches

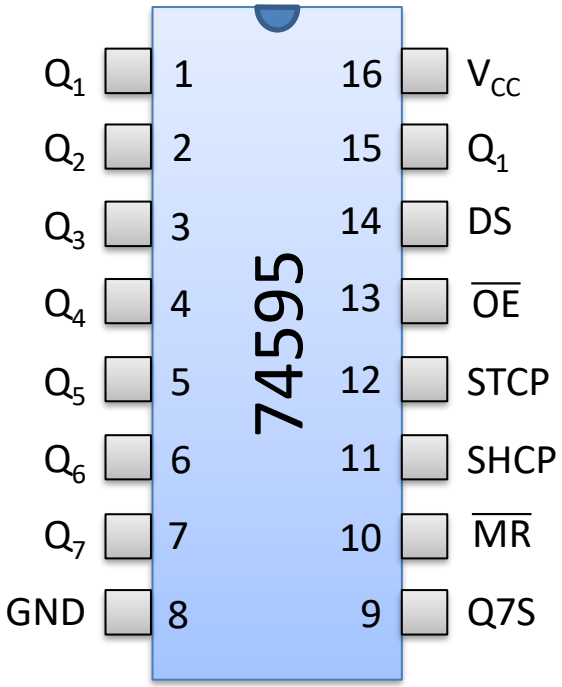


Shift Registers (5)

- 74595 – 8-bit serial-in shift register



Block Diagram



Pin Configuration

Shift Registers (6)

- 74595 – 8-bit serial-in shift register (continued)

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{MR}$	10	master reset
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{OE}$	13	output enable input
DS	14	serial data input
V_{CC}	16	supply voltage

Shift Registers (7)

- 74595 – *8-bit shift register*; 3-state (finished)

State	Description	Meaning
L	Low voltage	Output: current source
H	High voltage	Output: current sink
Z	High Impedance	Off state, not connected